

AN1671

MC145170 PSpice Modeling Kit

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Device models and simulators such as PSpice can provide the circuit designer with a method of reducing the amount of time spent in the laboratory. The key is in developing the proper model. While the models used by the IC designer could be used for simulating the circuit designer's application, it is a cumbersome, inefficient and more often than not, an inaccurate method for analyzing the operation of the actual circuit. A better method is to devise a model, which performs to the specification for the IC and trust the IC designer to produce a device that conforms to the specification. In this manner, simpler, faster simulations can be made.

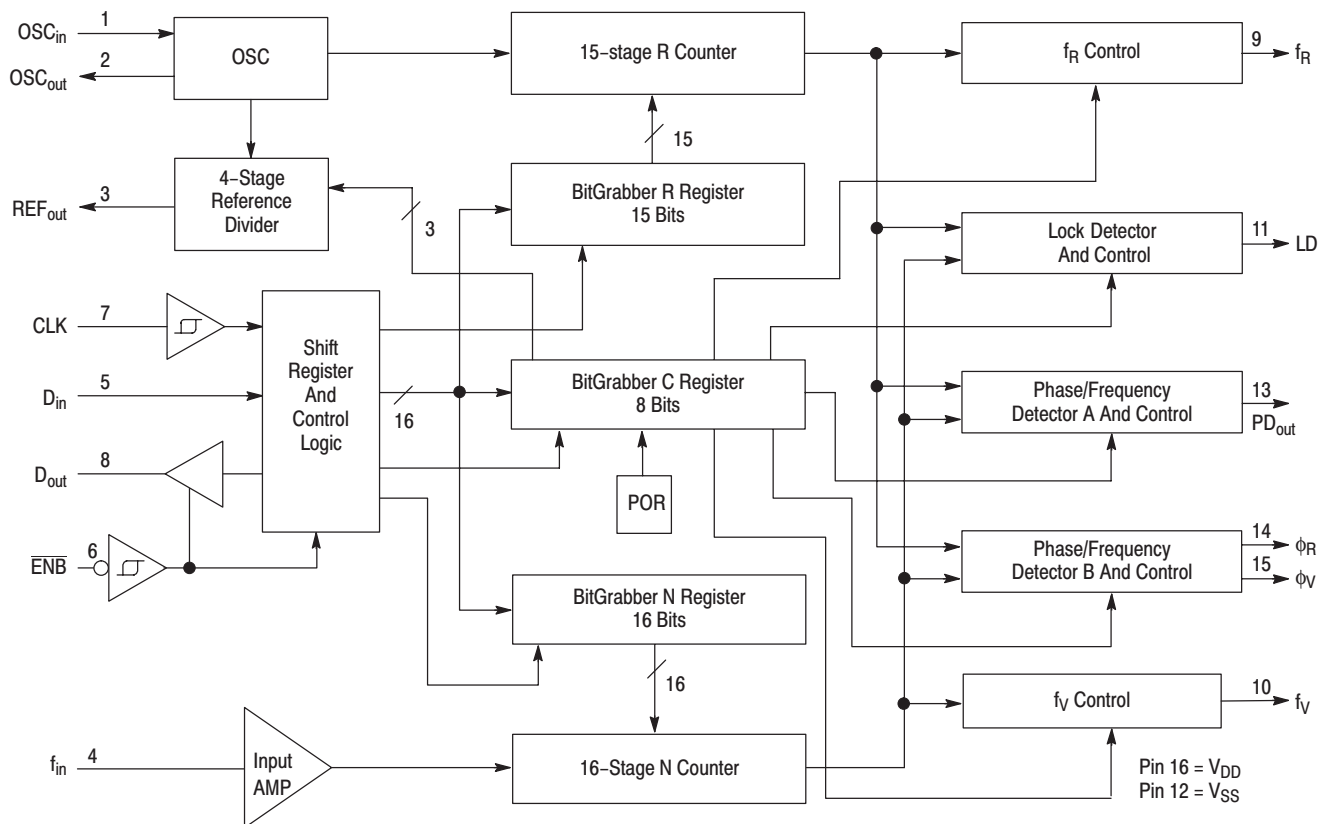
The following describes the application of this technique for the MC145170 PLL Frequency Synthesizer. PSpice Analog Behavioral Modeling is used to develop phase detector and VCO models. These are used to simulate open loop, closed loop and test purity of the VCO output. All simulations described below were performed at level 3.

Figure 1 shows the block diagram for the MC145170. The device is composed of serial communications hardware, a

reference oscillator, a phase detector and counters to divide the reference oscillator and input frequency. It is neither necessary nor practical to simulate the complete MC145170. To do so would only chew up a considerable amount of computer time and generate unmanageable data files. Since the simulator must calculate the conditions for each node for every step in the simulation, reducing the circuitry to the minimum required to obtain the desired results is not only attractive but also necessary.

The serial communications hardware establishes the operating conditions for the device but plays no active part in the operation of the PLL so it is not necessary for either closed loop or open loop analysis. The counters can also be considered as not essential to the operation of the loop if the correct model for the circuit is used. By including the divide ratio into the design of the VCO model and choosing the reference input to equal the phase detector frequency, the counters can be eliminated from the simulation. It may be desirable to simulate the oscillator operation but this can and should be done separate from the loop simulation.

Figure 1. Block Diagram



AN1671

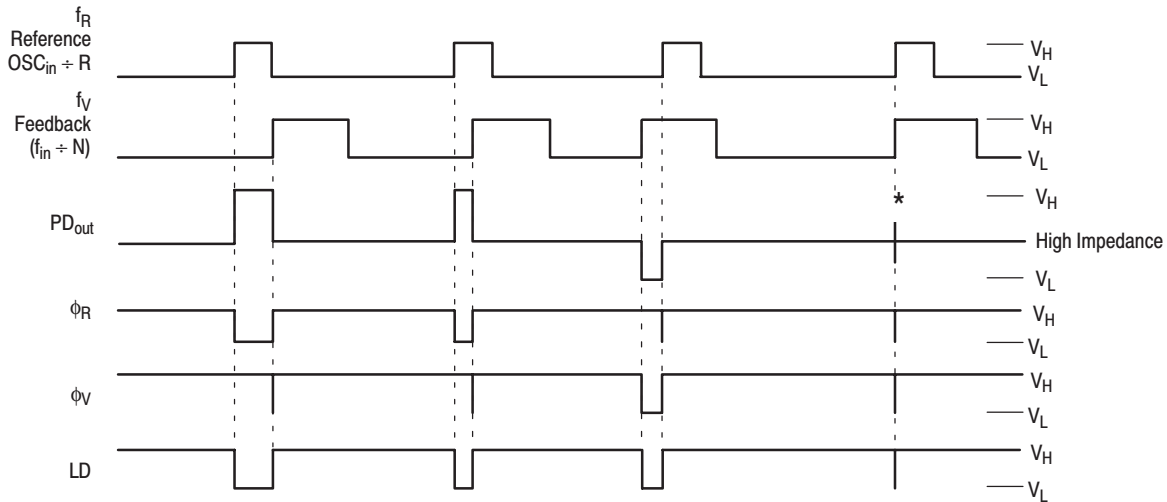
To simulate the operation of the PLL loop, we need only a model for the phase detector, a model for the VCO and the loop filter. The reference frequency is the frequency of the oscillator divided by the value programmed into the R counter. Rather than overloading the circuit simulation with a higher frequency followed by a counter, the reference frequency is used directly. In the same manner, the input amplifier and N counter can be folded into the model for the VCO.

Phase Detector Model

Figure 2 shows the input and output signals for the MC145170 phase detector. To accurately simulate the operation of the phase detector, it is necessary for the model to duplicate the output signals shown for the given input

signals. PhiR produces an output pulse when the reference signal leads the signal from the VCO with a pulse width equal to the amount of lead. PhiV produces the reverse condition and results from the reference signal lagging the feedback from the VCO. PD_{out} is the summation of PhiR and PhiV with the PhiR component driving positive and PhiV driving negative and high impedance between pulses. LD is also a summation but without the high impedance state. When either PhiR or PhiV is representing a non-zero lead or lag, the other will generate a pulse of minimum width. Both outputs will generate a minimum width pulse when locked. The minimum width of the output pulse is specified in the MC145170 data sheet and is 50 ns typical.

Figure 2.



V_H = High voltage level

V_L = Low voltage level

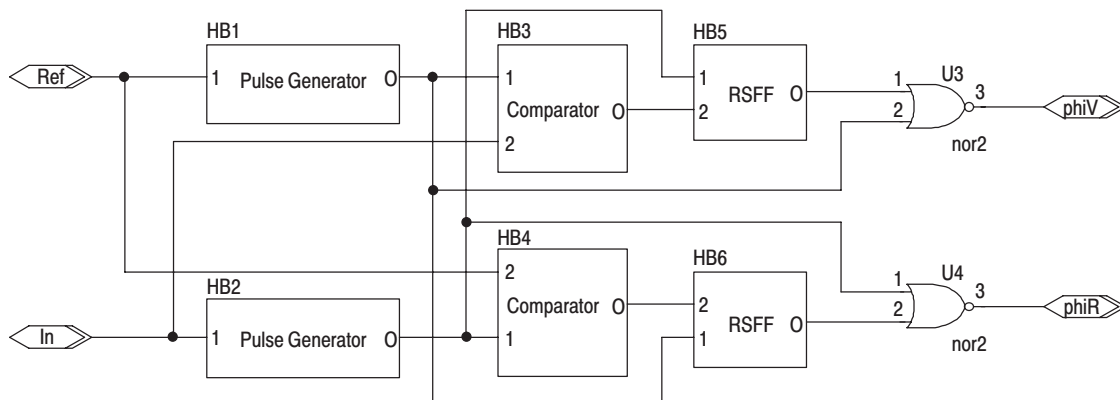
*At this point, when both f_R and f_V are in phase, both the sinking and sourcing output FETs are turned on for a very short interval.

NOTE: The PD_{out} generates error pulses during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor. PD_{out}, phi_R, and phi_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.

The block diagram for a model for the phase detector is shown in Figure 3. Two pulse generators produce narrow pulses coincident with the leading edges of In and Ref. The pulse generated from Ref is compared with In to determine if it leads or lags and the pulse generated from In is compared

with Ref. These signals drive the RS flip-flops which generate the basic correction signals. Since the model would generate no output when the circuit is locked, the NOR gates are added so the pulses are present in the output.

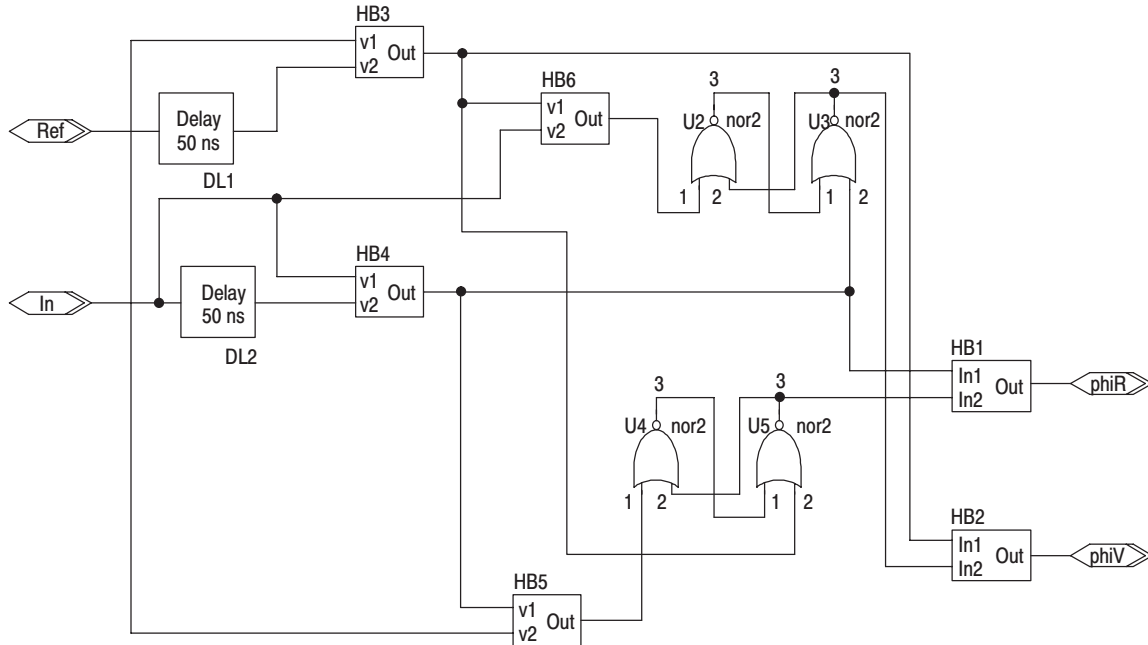
Figure 3.



The basic phase detector is shown in Figure 4. HB3, HB4, HB5 and HB6 all use the function shown in Figure 5. HB1 and

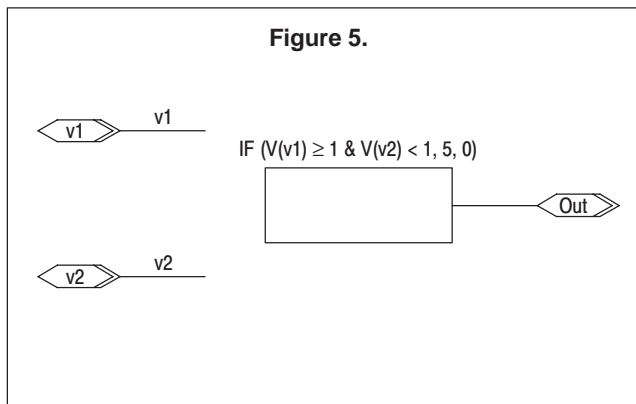
HB2 are behavioral implementations of a NOR gate (Figure 6).

Figure 4.



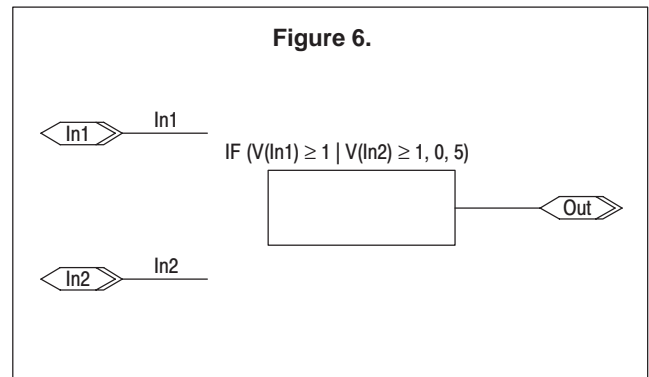
The circuit in Figure 5 performs both an AND operation and an inverter operation in one function. When used as HB3 and HB4, the output of the delay element is inverted and ANDed with the undelayed input. The result is a pulse whose width is equal to the value of the delay. As HB5 and HB6, the input signal (In or Ref), is inverted and compared with the corresponding pulse to determine if it leads or lags.

for each cycle of In and resets the RSFF to 0, terminating the pulse and holding the output of U3 at 0 for conditions where Ref does not lead In.



The output of HB3 is a pulse occurring at the rising edge of the Reference clock input. The output of HB4 is a similar pulse occurring at the rising edge of In. HB6 compares the output pulse of HB3 with In to determine if it leads In. If Ref leads In, then HB6 will generate a pulse at its output. If Ref lags In, the output of HB6 will be zero. In the same manner, HB5 generates a pulse when In leads Ref.

An RS flip-flop is used to generate the lead and lag pulses. HB6 sets the RSFF U2/U3 and the output of HB4 resets the RSFF. The output of U3 is a pulse whose width equals the amount of lead of Ref over In. HB4 outputs a pulse



The RSFF formed by U4/U5 performs the same function for In leading Ref. When In leads Ref, HB5 generates a pulse setting the U4, U5 RSFF. HB3 resets this FF coincident with the rising edge of Ref.

To fully emulate the operation of the MC145170 phase detector, the pulses must be present in the output. This is the purpose of HB1 and HB2. By adding the corresponding pulse to the outputs of the RSFFs, the operation of the phase detector has been emulated.

For best performance, the output of the phase detector model should look like the output of the phase detector in the MC145170. This can be accomplished by adding transistor models that represent those used in the MC145170. For applications using the PhiR and PhV outputs, Figure 7 can be used. For applications using PD_{Out}, use the circuit shown in Figure 8.

Figure 7.

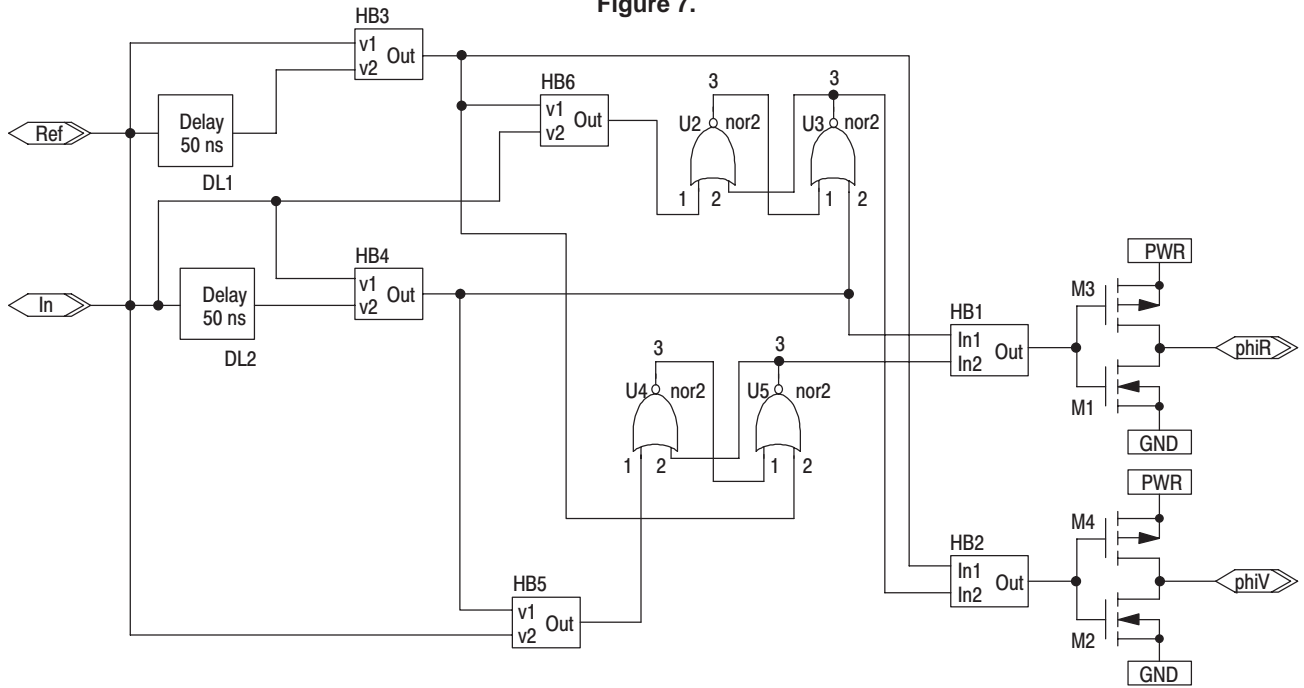
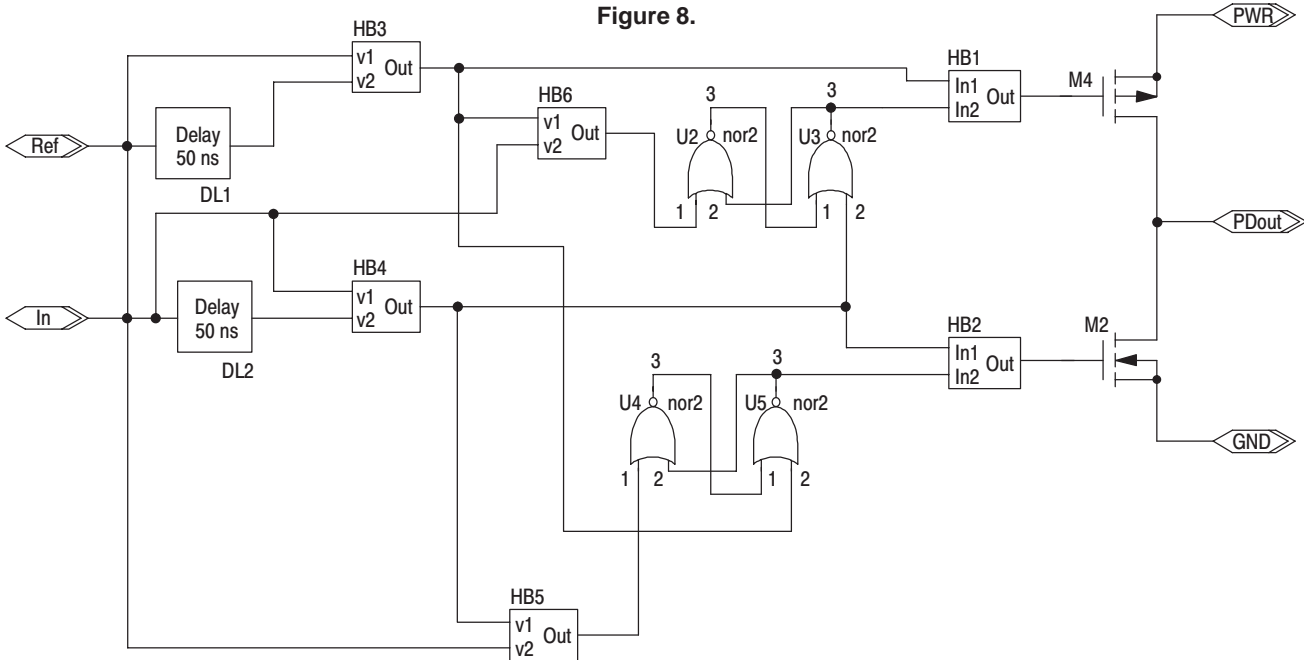


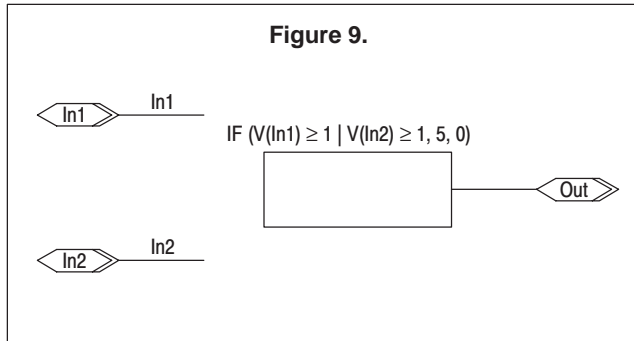
Figure 8.



To insure correct operation, HB1 and HB2 must be modified for each variation in configuration. For example, To insure the correct polarity for the output pulses, R and V outputs must reflect the correct polarity. This is achieved by the IF statement of HB1 and HB2. For applications where the behavioral gates drive the loop filter, the equation is as shown

in Figure 6. When the transistor buffer/inverters are added, the circuit must be modified to produce the correct polarity output, Figure 9.

Similar changes must be made when using the PD_{out} model. HB1 is represented by the circuit in Figure 9 and HB2 is represented by the circuit in Figure 6.



The typical operation model parameters for transistors used in the phase detector of the MC145170 are listed at the end of this paper. For NRD and NRS, use 4/210 for the pmos in the PDout driver, 4/66 for the nmos in the PDout driver, 4/300 for the pmos in the phiV and phiR buffers and 4/120 for the nmos in the phiR and phiV buffers. M can be used to establish the desired output drive of the transistors (from the MC145170 specification).

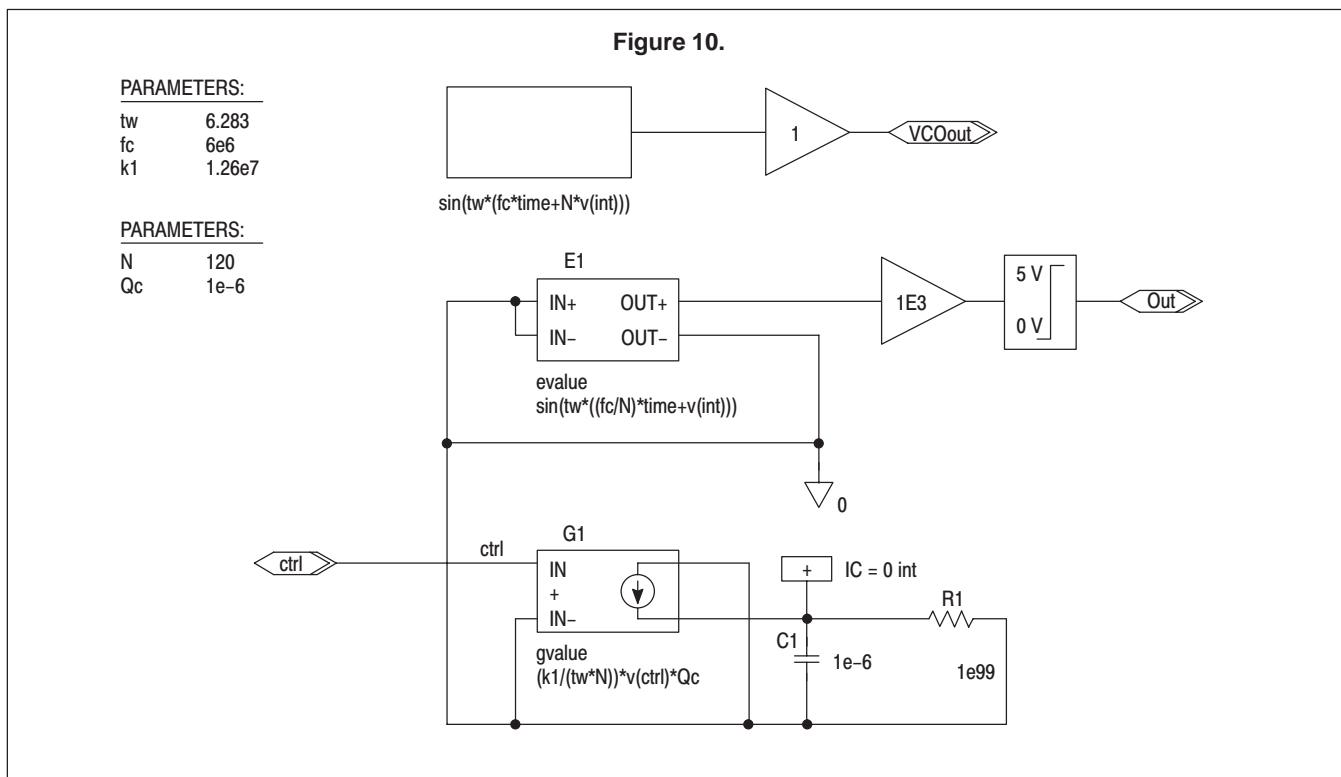
The operation of the phase detector can be simulated for different limits specified in the data sheet by modifying M for the output transistors and the adjusting the value of the delay element. For simulating devices with a specific minimum

pulse width, set the delay to the desired value. To observe the effect of changing transistor drive levels, set M appropriately.

Additional Modifications

The examples shown below can be simulated using MicroSim PSpice. In addition, the evaluation version of PSpice can also be used for simulation if appropriate adjustments to the models are made. These changes are only two. The libraries provided with the evaluation PSpice program do not include the primitive logic gates or the delay element. They do however contain several of the "7400" models which can be used for this application. The 7407 model can be used to implement the delay component and the 7402 can be used for constructing the RSFF. While the 7407 needs to be modified for use as a delay element, the 7402 can be used as is or the "02" model can be edited to reduce the propagation delay to that more in line with the primitive NOR gate.

Two changes must be made to the 7407 to use it as a delay element. The 7407 model must be modified to eliminate the "open collector" reference and the "07" model must be modified to contain the correct delay information. This can be done to the existing model or the 7407 and 07 models can be copied to the user library, renamed and modified to provide the special delay element. A simple text editor can be used to edit the device models.



Modeling the VCO

The VCO (Figure 10) is also modeled using Analog Behavioral Modeling. The model used in the following examples assumes a linear response however the control voltage equation can be modified as desired. The circuit is modeled as a sine generator controlled by the control voltage. The sine generator can be modeled using the EVALUE function or the ABM function. In Figure 10, the

EVALUE function is used to generate the divided output and the ABM function is used for the undivided output. Either the GVALUE or the ABM/I function can be used for the control voltage.

The equation for the generator is:

$$e = \sin(tw * ((fc/N) * time + v(int)))$$

AN1671

f_c is defined as the output frequency when the control voltage is zero. This is the expected VCO frequency before frequency division. For the purpose of simulation, the counter value, N , has been written into the equation to insure the correlation between the modeled circuit and the mathematical loop filter calculations. tw is pi times two; additional decimal places can be added as needed. $v(int)$ is the control voltage effect and is defined in these examples as:

$$v(int) = (k1 / (tw * N)) * v(cntl) * 1e-10.$$

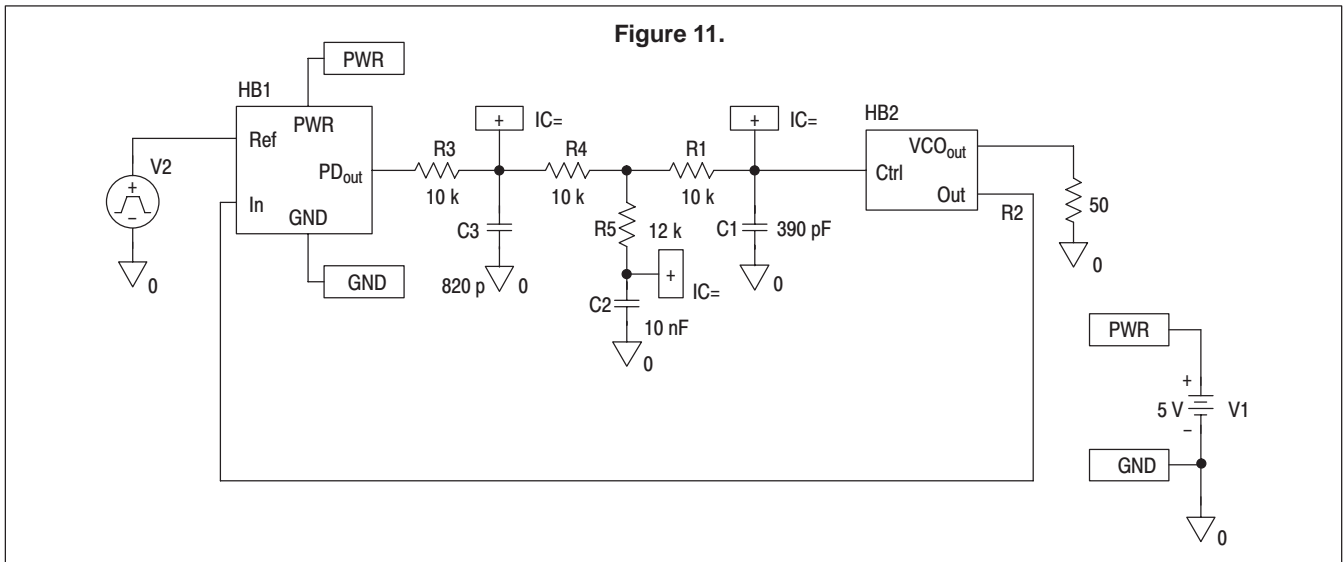
The value $C1$ in the schematic of the VCO can be arbitrarily changed however the value must match that of Q_c . Q_c determines the value of the current to be integrated by the capacitor $C1$. $R1$ is arbitrarily set to $1e99$ and is not an active part of the circuit however it must be included to prevent open pin errors from the PSpice software. The $GVALUE$ function is used to perform the generation of $v(int)$. There is some interaction between the integrator, ($GVALUE$ output and $C1$) and $R1$. $V(int)$ is a continuous ramp that is loaded by the resistance of $R1$. Unless the $GVALUE$ output current is sufficiently large for the value chosen for $R1$, the VCO control voltage required to maintain lock will increase throughout the simulation producing nonlinear operation. Modifications to the circuit can be performed either by changing the values in the parameter list or for major changes to the VCO characteristics, the equations for the sine generator or control voltage can be altered.

The output of the sine generator is amplified by 1000 to produce a sharp rise/fall time and the output limited to swing between the values of zero volts and +5 volts to convert it to a digital output. The resultant circuit/symbol accepts a voltage input from the loop filter and produces a square wave output at the desired frequency. This frequency should be chosen to represent the frequency present at the output of the N counter within the MC145170.

The second output represented by the ABM function is a sine wave output of the frequency expected from the actual VCO. The primary purpose of this output is to allow full frequency simulation for spectrum analysis. By running a transient analysis of sufficient time, it is possible to determine spur content and level. If sufficient resolution is used in the simulation, the PSpice probe FFT transform can be used to provide the typical spectrum analyzer display.

Example

Design a PLL frequency synthesizer circuit to generate an output stepping from 10 MHz to 12 MHz in 100 KHz increments. In this example, (Figure 11), with an output frequency of 10 MHz, N is chosen to be 100 and $V2$ is set for a step frequency of 100 KHz. The loop filter is (B) shown in the Phase-Locked Loop-Low Pass Filter Design section of the MC145170 data sheet. The series resistance has been split and C_c ($C3$ in Figure 11), inserted and additional filtering ($C1$, $R1$), added.



The performance of the VCO chosen for this application is shown in Figure 12. The VCO gain may be obtained from the relationship between the delta of f_{VCO} and the delta of v_{VCO} at the nominal operating frequency. Limiting operation to below 15 MHz will keep the gain linear enough to fit the model. If the output is to be operated at near 10 MHz, from the graph

$$KVCO = 2 * \pi * \Delta(f_{VCO}) / \Delta(v_{VCO}) = 1.27e7 \text{ rad/sec/V}$$

The phase detector gain is given by the MC145170 data sheet as

$$K\phi = VDD / 4 * \pi \text{ volts per radian for } PD_{out}.$$

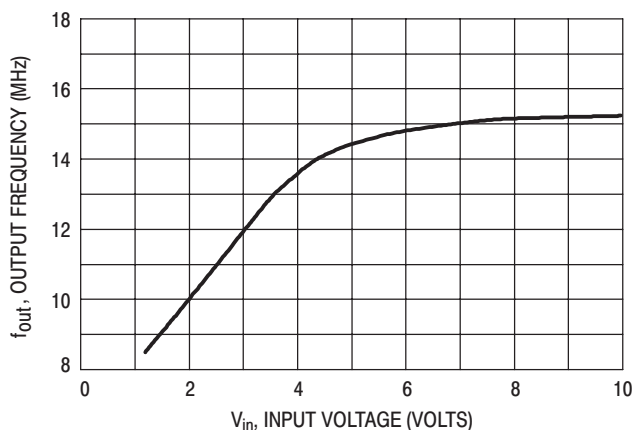
Letting

$$\omega_n = 2 * \pi * fR / 50 = 12,566 \text{ rad/s}$$

the loop filter values can be calculated. Choosing $C = 10 \text{ nf}$, the value for $R1 + R2$ can be calculated.

$$(R1 + R2) = K\phi * KVCO / N * C * (\omega_n)^2 \sim 32k$$

Figure 12.



For a damping factor of 0.8,

$$R2 = (0.8/0.5 * \omega_n - N/K\phi * KVCO)/C \sim 12k$$

$$R1 = (R1+R2) - R2 = 20 \text{ k ohm.}$$

If C_c is chosen such that $C_c = 4/(R1\omega RC)$ where ωRC is the filter cutoff frequency, then

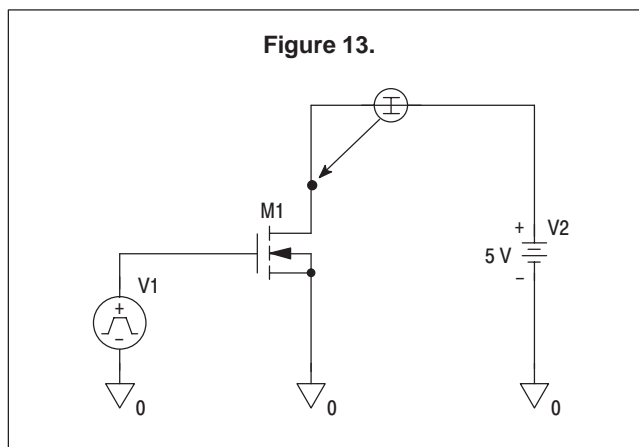
$$C_c \sim 820\text{pf.}$$

(Refer to the AN1207 application note: formulas 8, 9 and 10.)

If additional filtering is needed, equation 11 from the AN1207 application note may be used to determine the capacitance value for an additional filter element. If the resistance of $R1$ is chosen as 10 k, the value of $C1$ is

$$C1 = 1/\omega RC * R1 \sim 390\text{pf.}$$

Figure 13.



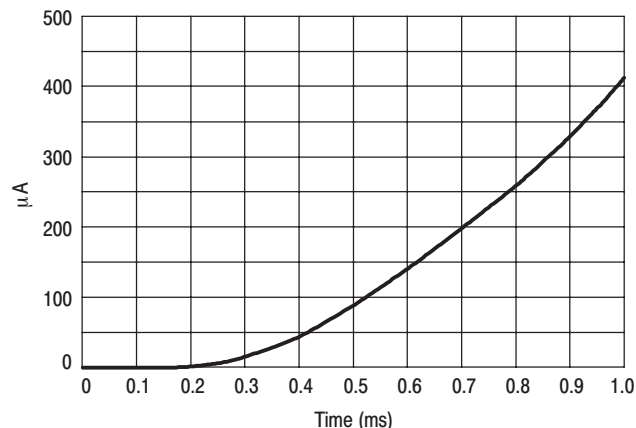
Simulation

The Phase Detector used in Figure 11 is the version shown in Figure 8. Before simulating, the delay should be set to obtain the desired minimum pulse width and the output transistors should be configured for the correct NRD, NRS and M. The VCO model is shown in Figure 10 and is configured for this example.

The transistor characteristics can be examined by running a quick simulation of the circuit shown in Figure 13. Access the attributes menu for the NMOS transistor and select NRD or NRS. Set both values to $4/66$ ($6.0606e-2$). Set VPULSE to

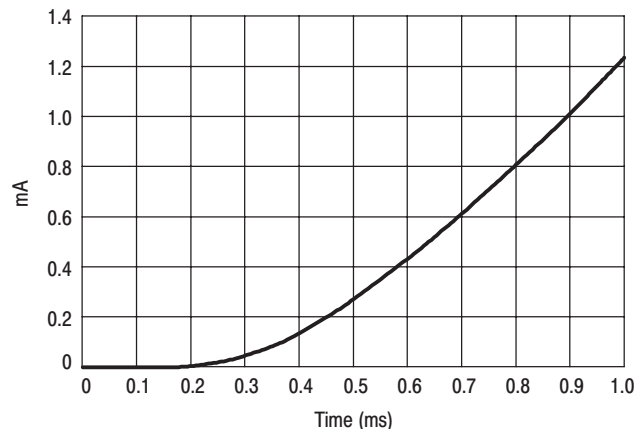
ramp from zero to 5 V. Place a current marker on the drain of the NMOS transistor and simulate (1 ms is adequate). The result is shown in Figure 14.

Figure 14.



M was left at the default setting of one for this run. By specifying a specific number for M, the current shown in Figure 14 will be multiplied by this number. For example, if we set M at three, the transfer characteristics will be as shown in Figure 15.

Figure 15.



The desired output drive can now be obtained by adjusting the value for M. The same procedure is used for the PMOS transistor except the value for NRD and NRS is $4/210$ ($1.9048e-2$), and M should be approximately twice that used for the NMOS transistor for a balanced output.

Before beginning the simulation, the three initial conditions (IC=), should be set and reference oscillator should be set. The initial condition values can be set to zero for an initial simulation then reset later to the values desired for later simulations. The reference oscillator, V2, is a VPULSE function with V1=zero, V2=5 V, tr, tf, pw and per set to produce a 100 KHz square wave. By referring to Figure 12, we can expect the control voltage at lock to be approximately 2 V. Since the linear portion of the VCO characteristics curve is approximately 8 MHz to 15 MHz, we are interested in the circuit activity for control voltages between 1.5 V and 3.5 V. Except for examining performance at startup, we will set IC to some value between these values.

AN1671

The exact value of the initial condition depends of what condition is being simulated. For example, suppose we wish to observe the loop performance for the VCO output stepping from 10 MHz to 12 MHz (the range of operation we have chosen). First, we modify the VCO model to change N to 120,

set each IC flag to 2 V and run the simulation. The value 2 V is approximately the control voltage required to produce a VCO output of 10 MHz. The initial conditions will then reflect a beginning condition of 10 MHz followed by a step to 12 MHz. Figure 16 shows the 1.5 ms simulation run.

Figure 16.

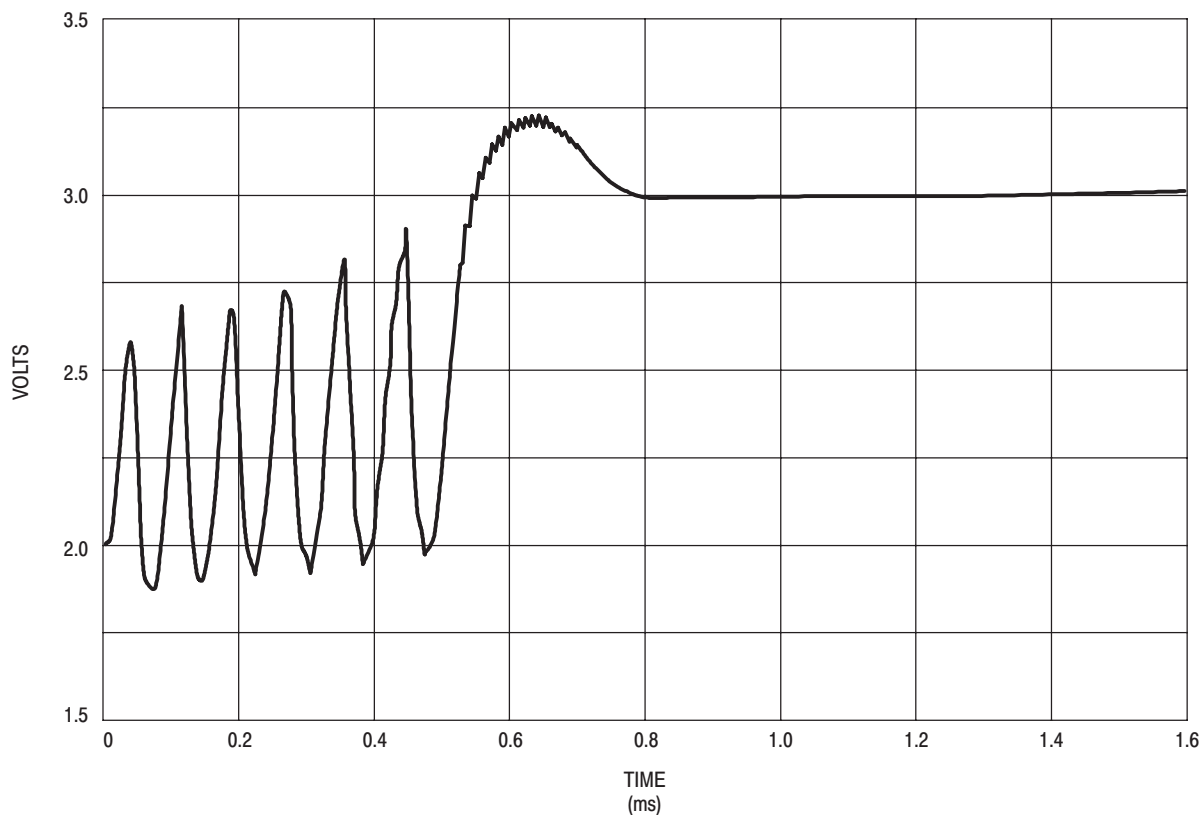


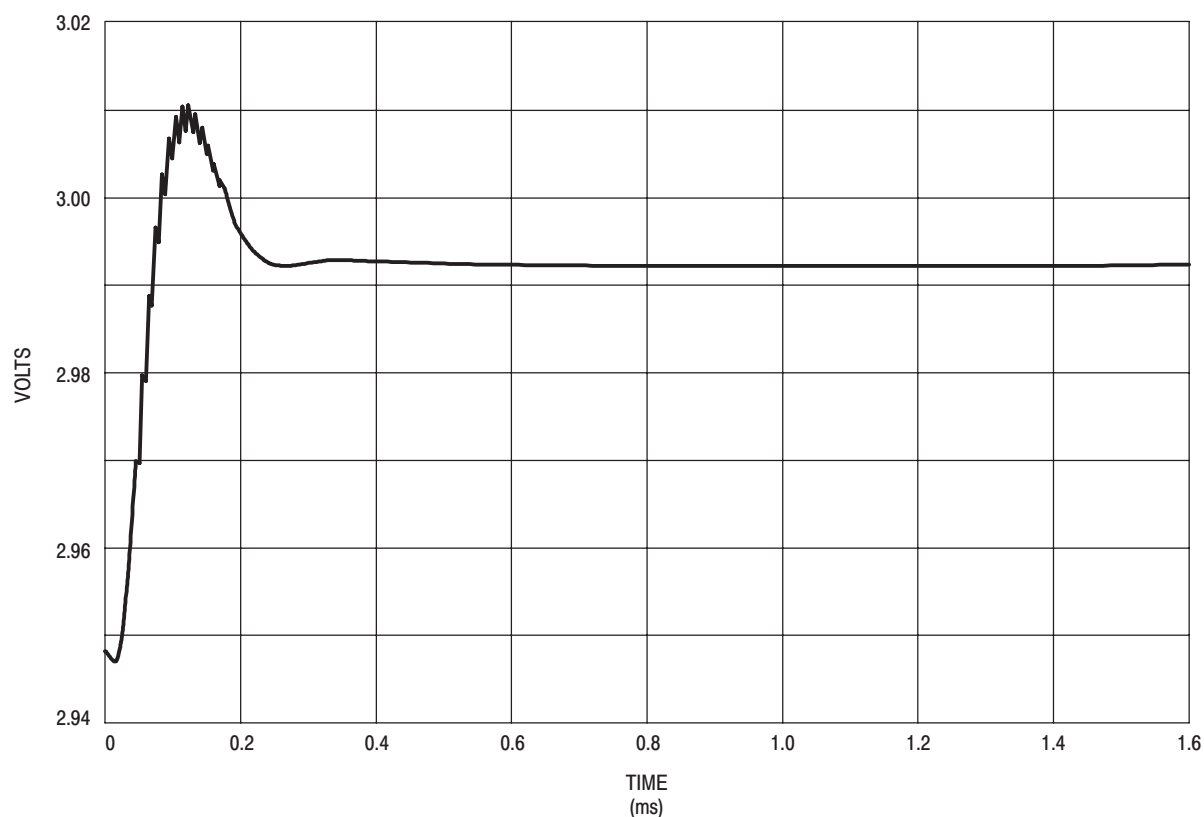
Figure 17 shows the step response for one 100 KHz step. Referring to the chart in Figure 12, with the VCO model set up for N = 120,

$$(dF)/dV = 2 \text{ MHz per volt.}$$

$$100 \text{ KHz}/2 \text{ MHz per volt} = 5e-2 \text{ volt per } 100 \text{ KHz step.}$$

If the initial conditions are set to IC = 2.95 V, the circuit will simulate the VCO stepping from 11.9 MHz to 12 MHz. The response of the loop filter is viewed at the input to the VCO. It can be seen that the circuit is locked and stable at t = 0.4 ms.

Figure 17.

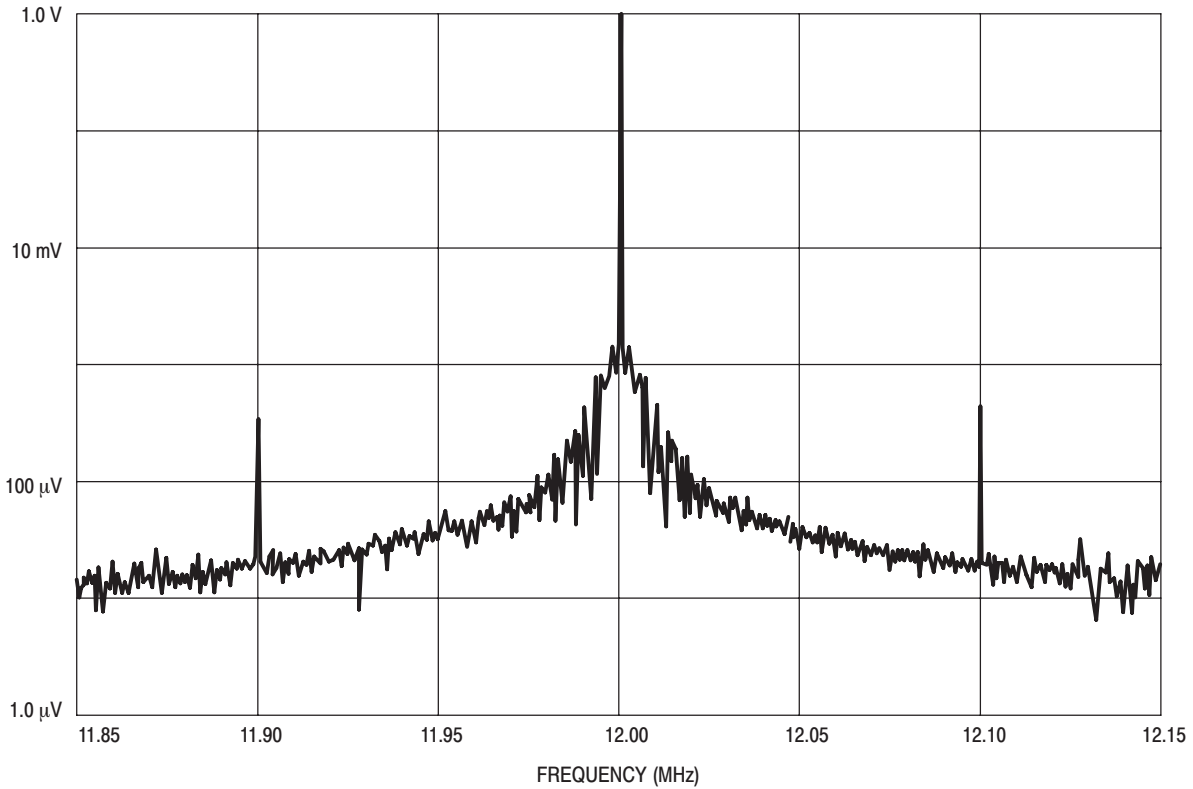


To analyze the circuit for spur amplitude on the output of the VCO, the simulation must contain adequate simulation time. In addition this simulation must contain data for stable operation only and must be of sufficient resolution. At least three samples (four is recommended), per cycle should be made. This is achieved by setting step ceiling in the analysis menu. For example, if the VCO output is 12 MHz, the step ceiling should be set to about 10 ns. 2.5 ms provide an adequate number of samples for a clean display.

To insure that only stable data is obtained from the simulation, the initial condition settings are set to reflect the voltages present after the circuit is stabilized. These can be calculated or the simulation run long enough to stabilize and the values measured using a marker. There will be some

degree of uncertainty for the values at the phase detector output since these contain a significant amount of the 100 KHz switching components. An approximate value is sufficient as the print delay can be used to eliminate any residual settling. Setting IC = 3 V for all three initial conditions and using a print delay of 0.5 ms, sufficient samples are obtained for the display. The high frequency output of the VCO is measured and the FFT function is used to obtain a time/amplitude plot. Limiting the span to ± 150 KHz with logarithmic vertical axis, the display is shown in Figure 18. The amplitude of the spur at 12.1 MHz is measured as 0.454 mv. The maximum amplitude of the primary is 0.954 V giving a suppression of 66 db for this implementation.

Figure 18.

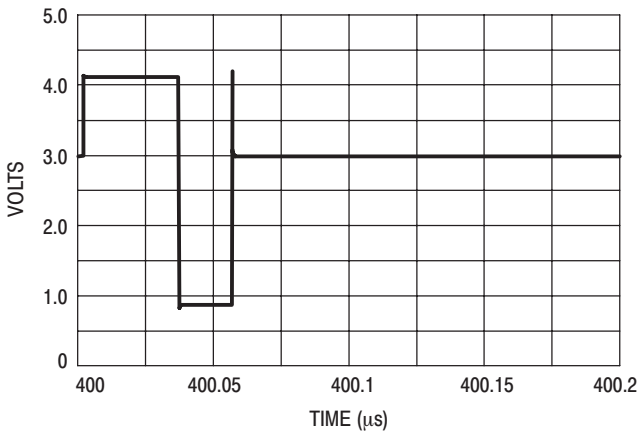


Circuit Analysis

PSpice may also be used for analyzing existing circuits. By measuring conditions in operating circuits and comparing the results to simulations of the schematic representation of the circuit, values for parameters such as parasitic capacitance and inductance can be obtained.

If the circuit in Figure 11 is simulated and the output of the phase detector, PD_{out}, is displayed, the result will be as shown in Figure 19.

Figure 19.



If the actual circuit is measured, the result varies considerably from what is shown in Figure 19. The reason for the difference is the same whenever any simulation fails to track the actual circuit. It is an incomplete model. Unless the model describes all parameters well enough to produce the desired results, differences between the actual circuit and the modeled circuit occur.

This example however is quite easy to correct. Normally, parasitic components are not drawn on schematics. The engineer is supposed to recognize that they exist and modify his design and procedures accordingly. In this case, the problem is the inductive component of the PCB trace connecting the phase detector output, the loop filter components and the VCO together and stray capacitance from pads and jumpers. In an actual implementation of this circuit (the MC145170EVK PCB), several jumpers are used to select a variety of loop configurations. The contributions of these jumpers and the PCB traces affect the phase detector output. If the circuit is modified (Figure 20), to include the stray components (along with scope probe loading) and the simulation rerun, the result tracks the actual circuit quite closely (Figure 21).

Figure 20.

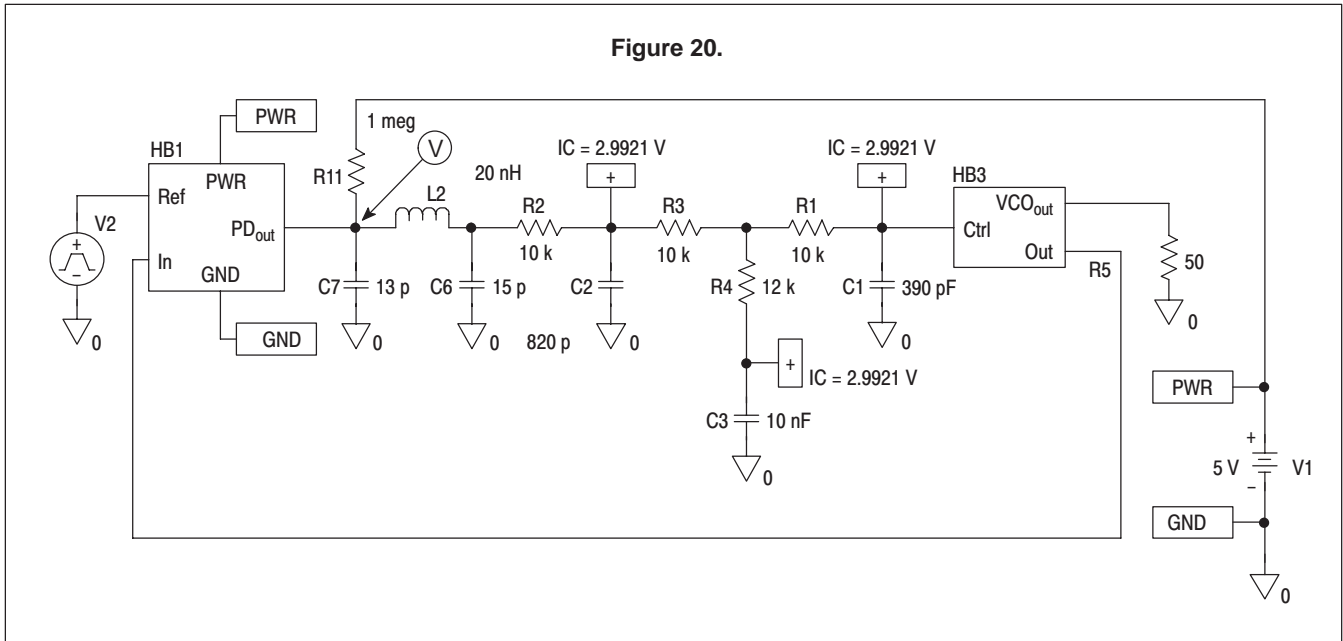
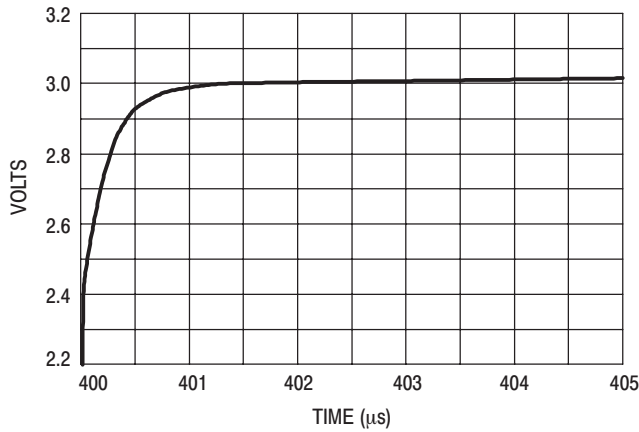


Figure 21.



Computing Resources

PSpice and other Spice simulators incorporating full Berkeley Spice compatibility require significant computing power. When running PSpice on the PC, a Pentium processor with RAM capability equal to or greater than that recommended by MicroSim should be used. In addition, large data files are generated when simulating high resolution, long period transient analysis. Sufficient disk space should be provided if spectrum analysis of the VCO is to be performed. A gigabyte-sized drive is not too large for this type of analysis.

Conclusion

Although PSpice is not blinding fast for some analysis types and large data files can fill a drive if not properly managed, simulating PLL circuits can provide the circuit designer fast design and verification of synthesizer circuits. While there is no substitute for building and testing the actual circuit, many what-if conditions and basic design questions can be answered by simulating first.

AN1671

Attachment

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**++ SPICE MODEL LEVEL 3 PARAMETERS FOR HCMOS
** DATA FOR THIS DIE: RSH_N=78 OHMS/SQ. TYP, RSH_P=128 OHMS/SQ. TYP.
** LEFF_N = 0.84UM, LEFF_P = 0.90UM.
** WEFF_N = 1.07UM, WEFF_P = 1.04UM.
** TARGETS FOR THIS PROCESS: LEFF_N = 0.90UM, 1-SIGMA = 0.075UM
** LEFF_P = 0.90UM, 1-SIGMA = 0.075UM
** WEFF_N = 1.00UM, 1-SIGMA = 0.10UM
** WEFF_P = 1.00UM, 1-SIGMA = 0.10UM
** ODIFF_N (TOTAL) = 0.08UM TYP. ODIFF_P (TOTAL) = 0.06UM TYP.
** LYNN RILEY 2/7/91
*LEFF BASED ON EQUATION: LEFF = LDASH - 2*LD + DL
*WEFF BASED ON EQUATION: WEFF = WDASH + DW
**@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
** TYPICAL CASE
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*
LIB TYP
.MODEL N1 NMOS
+ LEVEL = 3
+ NSS = 0.00000E+00 VTO = 8.30000E-01 TOX = 2.25000E-08
+ XJ = 1.66632E-07 LD = 0.04000E-06 RSH = 6.40359E+02
+ NSUB = 1.82429E+16 NFS = 1.26963E+11 UO = 5.95254E+02
+ VMAX = 1.86907E+05 DELTA = 8.22502E-01 THETA = 5.77858E-02
+ ETA = 2.19310E-02 KAPPA = 2.60564E-01
+ CGSO = 6.133E-11 CGDO = 6.133E-11 CGBO = 2.62990E-10
+ CJ = 2.59E-04 CJSW = 2E-10 PB = 0.811
+ MJ = 0.36 MJSW = 0.31 TPG = 1
+ DW = -0.48000E-06 DL = -0.50000E-06
+ XQC = 1
*
.MODEL P1 PMOS
+ LEVEL = 3
+ NSS = 0.00000E+00 VTO = -9.70000E-01 TOX = 2.25000E-08
+ XJ = 6.09033E-08 LD = 0.03000E-06 RSH = 2.20074E+03
+ NSUB = 2.22297E+16 NFS = 1.02169E+12 UO = 1.64004E+02
+ VMAX = 1.59023E+07 DELTA = 6.46809E-01 THETA = 1.03214E-01
+ ETA = 2.00000E-02 KAPPA = 5.06893E-02
+ CGSO = 4.60E-11 CGDO = 4.60E-11 CGBO = 2.62990E-10
+ CJ = 4.25E-04 CJSW = 2E-10 PB = 0.772
+ MJ = 0.48 MJSW = 0.20 TPG = -1
+ DW = -0.48000E-06 DL = -0.52000E-06
+ XQC = 1
ENDL TYP
*
**@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
** 63% UDR MOS2 N-WELL
** BEST CASE SPEED
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+ LEVEL = 3
+ NSS = 0.00000E+00 VTO = 6.30000E-01 TOX = 1.90000E-08
+ XJ = 1.66632E-07 LD = 0.04000E-06 RSH = 6.40359E+02
+ NSUB = 1.82429E+16 NFS = 1.26963E+11 UO = 5.95254E+02
+ VMAX = 1.86907E+05 DELTA = 8.22502E-01 THETA = 5.77858E-02
+ ETA = 2.19310E-02 KAPPA = 2.60564E-01
+ CGSO = 7.263E-11 CGDO = 7.263E-11 CGBO = 1.11890E-10
+ CJ = 2.59E-04 CJSW = 2E-10 PB = 0.811
+ MJ = 0.36 MJSW = 0.31 TPG = 1
+ DW = -0.18000E-06 DL = -0.72500E-06
+ XQC = 1
*
.MODEL P1 PMOS
+ LEVEL = 3
+ NSS = 0.00000E+00 VTO = -7.70000E-01 TOX = 1.90000E-08
+ XJ = 6.09033E-08 LD = 0.03000E-06 RSH = 2.20074E+03
+ NSUB = 2.22297E+16 NFS = 1.02169E+12 UO = 1.64004E+02
+ VMAX = 1.59023E+07 DELTA = 6.46809E-01 THETA = 1.03214E-01
+ ETA = 2.00000E-02 KAPPA = 5.06893E-02
+ CGSO = 5.447E-11 CGDO = 5.447E-11 CGBO = 1.11890E-10
+ CJ = 4.25E-04 CJSW = 2E-10 PB = 0.772
+ MJ = 0.48 MJSW = 0.20 TPG = -1
+ DW = -0.18000E-06 DL = -0.74500E-06
+ XQC = 1
ENDL BCS
```

```

*
**@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
** 63% UDR MOS2 N-WELL
** WORST CASE SPEED
**@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
*

```

```

LIB WCS
.MODEL N1 NMOS
+ LEVEL = 3
+ NSS = 0.0000E+00 VTO = 1.0300E+00 TOX = 2.6000E-08
+ XJ = 1.6663E-07 LD = 0.0400E-06 RSH = 6.4035E+02
+ NSUB = 1.8242E+16 NFS = 1.2696E+11 UO = 5.9525E+02
+ VMAX = 1.8690E+05 DELTA = 8.2250E-01 THETA = 5.7785E-02
+ ETA = 2.1931E-02 KAPPA = 2.6056E-01
+ CGSO = 5.308E-11 CGDO = 5.308E-11 CGBO = 5.9803E-10
+ CJ = 2.59E-04 CJSW = 2E-10 PB = 0.811
+ MJ = 0.36 MJSW = 0.31 TPG = 1
+ DW = -0.7800E-06 DL = -0.2750E-06
+ XQC = 1
*

```

```

.MODEL P1 PMOS
+ LEVEL = 3
+ NSS = 0.0000E+00 VTO = -1.1700E+00 TOX = 2.6000E-08
+ XJ = 6.0903E-08 LD = 0.0300E-06 RSH = 2.2007E+03
+ NSUB = 2.2229E+16 NFS = 1.0216E+12 UO = 1.6400E+02
+ VMAX = 1.5902E+07 DELTA = 6.4680E-01 THETA = 1.0321E-01
+ ETA = 2.0000E-02 KAPPA = 5.0689E-02
+ CGSO = 3.981E-11 CGDO = 3.981E-11 CGBO = 5.9803E-10
+ CJ = 4.25E-04 CJSW = 2E-10 PB = 0.772
+ MJ = 0.48 MJSW = 0.20 TPG = -1
+ DW = -0.7800E-06 DL = -0.2950E-06
+ XQC = 1
*

```

```

ENDL WCS
*
**@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
** 63% UDR MOS2 N-WELL
** WORST CASE VOH (BEST N/WORST P)
**@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
*

```

```

LIB VOH
.MODEL N1 NMOS
+ LEVEL = 3
+ NSS = 0.0000E+00 VTO = 6.3000E-01 TOX = 1.9000E-08
+ XJ = 1.6663E-07 LD = 0.0400E-06 RSH = 6.4035E+02
+ NSUB = 1.8242E+16 NFS = 1.2696E+11 UO = 5.9525E+02
+ VMAX = 1.8690E+05 DELTA = 8.2250E-01 THETA = 5.7785E-02
+ ETA = 2.1931E-02 KAPPA = 2.6056E-01
+ CGSO = 7.263E-11 CGDO = 7.263E-11 CGBO = 1.1189E-10
+ CJ = 2.59E-04 CJSW = 2E-10 PB = 0.811
+ MJ = 0.36 MJSW = 0.31 TPG = 1
+ DW = -0.7800E-06 DL = -0.7250E-06
+ XQC = 1
*

```

```

.MODEL P1 PMOS
+ LEVEL = 3
+ NSS = 0.0000E+00 VTO = -1.1700E+00 TOX = 1.9000E-08
+ XJ = 6.0903E-08 LD = 0.0300E-06 RSH = 2.2007E+03
+ NSUB = 2.2229E+16 NFS = 1.0216E+12 UO = 1.6400E+02
+ VMAX = 1.5902E+07 DELTA = 6.4680E-01 THETA = 1.0321E-01
+ ETA = 2.0000E-02 KAPPA = 5.0689E-02
+ CGSO = 5.447E-11 CGDO = 5.447E-11 CGBO = 1.1189E-10
+ CJ = 4.25E-04 CJSW = 2E-10 PB = 0.772
+ MJ = 0.48 MJSW = 0.20 TPG = -1
+ DW = -0.7800E-06 DL = -0.7450E-06
+ XQC = 1
*

```

```

ENDL VOH
*
**@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
** 63% UDR MOS2 N-WELL
** WORST CASE VOL (BEST P/WORST N)
**@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
*

```

```

LIB VOL
.MODEL N1 NMOS
+ LEVEL = 3
+ NSS = 0.0000E+00 VTO = 1.0300E+00 TOX = 2.6000E-08
+ XJ = 1.6663E-07 LD = 0.0400E-06 RSH = 6.4035E+02

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AN1671

```

+ NSUB   = 1.82429E+16 NFS     = 1.26963E+11 UO      = 5.95254E+02
+ VMAX   = 1.86907E+05 DELTA   = 8.22502E-01 THETA   = 5.77858E-02
+ ETA    = 2.19310E-02 KAPPA   = 2.60564E-01
+ CGSO   = 5.308E-11 CGDO     = 5.308E-11 CGBO     = 5.98030E-10
+ CJ     = 2.59E-04 CJSW      = 2E-10 PB          = 0.811
+ MJ     = 0.36 MJSW         = 0.31 TPG          = 1
+ DW     = -0.18000E-06 DL     = -0.27500E-06
+ XQC    = 1
*
.MODEL P1 PMOS
+ LEVEL  = 3
+ NSS    = 0.00000E+00 VTO     = -7.70000E-01 TOX     = 2.60000E-08
+ XJ     = 6.09033E-08 LD      = 0.03000E-06 RSH     = 2.20074E+03
+ NSUB   = 2.22297E+16 NFS     = 1.02169E+12 UO      = 1.64004E+02
+ VMAX   = 1.59023E+07 DELTA   = 6.46809E-01 THETA   = 1.03214E-01
+ ETA    = 2.00000E-02 KAPPA   = 5.06893E-02
+ CGSO   = 3.981E-11 CGDO     = 3.981E-11 CGBO     = 5.98030E-10
+ CJ     = 4.25E-04 CJSW      = 2E-10 PB          = 0.772
+ MJ     = 0.48 MJSW         = 0.20 TPG          = -1
+ DW     = -0.18000E-06 DL     = -0.29500E-06
+ XQC    = 1
ENDL VOL
**@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@

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